CLAIMS:

1. A gamma correction circuit for correcting a digital video signal, the circuit comprising:

a first lookup table (6) and a second lookup table (8) for storing discrete output intensity data and the associated slope data of a non-linear transfer function, respectively, for each of the discrete input video signal intensities,

an adder (10) having a first input connected to the output of the first lookup table (6),

a multiplier (12) having a first input connected to the output of the second look-up table (8),

characterized by a quantizer (4) for providing the most significant bits of the incoming video signal to address the first and second lookup tables (6, 8) and to transfer the corresponding output intensity data to the adder (10) and the associated slope data to the multiplier (12), the quantizer (4) transmitting the remaining least significant bits of the input video signal to the second input of the multiplier (12), the multiplier (12) multiplying the slope data with the remaining least significant bits and feeding the multiplication result to the second input of the adder (10), the adder (10) adding the output intensity data and the multiplication result to generate a corrected video signal.

2. A gamma correction circuit according to claim 1, wherein data of the transfer function stored in the first lookup table (6) and the second lookup table (8) approximate the gamma correction characteristic.

3. Gamma correction circuit according to claim 1, wherein the transfer function in the first lookup table (6) and the second lookup table (8) approximate a modified gamma correction characteristic, and wherein the signal generated by the adder (10) is converted in processing means (32-40) into an approximation of a fully gamma-corrected video signal.

4. Gamma correction circuit according to claim 3, the requested gamma correction characteristic being defined as $Y=X^{gamma}$, X being the uncorrected video signal, Y being the corrected video signal, gamma being the correction factor,
wherein the lookup tables (6, 8) approximate a transfer function $Y=X^{gamma/2}$,
wherein the processing means includes a squarer (34) which squares the signal received from the adder (10) to output a fully gamma-corrected video signal, corrected by the correction factor gamma.

5. Gamma correction circuit according to claim 1, wherein the lookup tables (6, 8) approximate a transfer function $Y=X^{gamma}$, and the adder (10) outputs the gamma-corrected video signal, if gamma is below a pre-given value, and wherein the lookup tables (6, 8) approximate a transfer function $Y=X^{gamma/2}$, and the processing means (32-40) outputs the gamma-corrected video signal, if gamma is above the pre-given value.

6. Gamma correction circuit according to claim 5, wherein the pre-given value of gamma is approximately 1.4.

7. Gamma correction circuit according to claim 1, the input video path being n bits wide, the internal path being (q+p) bits wide, and the output video path being r bits wide, $r \leq (q+p)$, wherein the circuit includes an error propagation circuit (60-70) at the output of the adder (10) and/or at the output of the processing means (32-40), M least significant bits of the gamma-corrected video signal of each pixel being delayed by one pixel and added to the gamma-corrected video signal of the following next pixel.

8. Gamma correction circuit according to claim 7, wherein $M \geq (q+p-r)$.

9. Gamma correction circuit according to claim 7, wherein the error propagation circuit (60-70) includes in series a second adder (62) and a second quantizer (64), the second quantizer (64) separating the M least significant bits of the gamma-corrected video signal and passing the M bits through a pixel delay (66) which delays the M bits by one pixel back to the second input of the second adder (62).

10. Gamma correction circuit according to claim 7, wherein the input video signal X at the input is n bits wide, the data of the transfer functions stored in the lookup tables (6,

8) being q bits data, the output of the first lookup table (6) being shifted to the left by p bits, so that (q+p) bits are fed to the first input of the adder (10), the multiplier (12) outputs a (q+p) bits signal to the second input of the adder (10) which outputs a (q+p) bit signal, or wherein the processing means (32-40) receives the (q+p) bit signal from the adder (10) and outputs a (q+p) bit signal, either the output of the adder (10) or the output of the processing means (32-40) being the gamma-corrected video signal, the signal passing an error propagation circuit (60-70) in which the M least significant bits of the gamma-corrected video signal of each video pixel are added to the gamma-corrected video signal of the next pixel and an r bits signal being output as noise shaped gamma-corrected video signal.

11. Gamma correction circuit according to claim 10, wherein the input video path is n bits wide, the output video path is r bits wide, n=10, p=4, q = 10, M = 9 to 4, r = 5 to 10, and $M \geq (q+p-r)$.